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Fee et al.

Serial No.: 09/933,297

Filed: August 20, 2001

For: QUAD FLAT NO-LEAD (QFN) GRID ARRAY PACKAGE, METHOD OF MAKING MEMORY MODULE AND COMPUTER SYSTEM INCLUDING SAME

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COMMUNICATION

Commissioner for Patents
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Sir:

Enclosed is a certified copy of priority document 200104675-4 filed August 6, 2001 for the above-referenced application.

Respectfully submitted,

Bradley B. Jensen
Registration No. 46,801
Attorney for Applicants
TRASK BRITT
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: January 29, 2003
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This is to certify that the annexed is a true copy of the following Singapore patent application as filed in this Registry.

Date of Filing	:	6 AUGUST 2001
Application Number	:	200104675-4
Applicant(s)	:	MICRON TECHNOLOGY, INC.
Title of Invention	:	QUAD FLAT NO-LEAD (QFN) GRID ARRAY PACKAGE, METHOD OF MAKING AND MEMORYMODULE AND COMPUTER SYSTEM INCLUDING SAME

Yoon Mun Kit
Assistant Registrar
for REGISTRAR OF PATENTS

PATENTS FORM 1

Rule 19

SINGAPORE
PATENTS ACT
(CHAPTER 221)
PATENTS RULES

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200104675-4

The Registrar of Patents
Registry of Patents

REQUEST FOR THE GRANT OF A PATENT
THE GRANT OF A PATENT IS REQUESTED BY THE UNDERSIGNED ON THE BASIS OF THE PRESENT APPLICATION

I. Title of Invention	**QUAD FLAT NO-LEAD (QFN) GRID ARRAY PACKAGE, METHOD OF MAKING AND MEMORY MODULE AND COMPUTER SYSTEM INCLUDING SAME**	
II. Applicant(s) (*See note 2*)	***(a) Name***	**MICRON TECHNOLOGY, INC.**
	Body Description/ Residency	**A CORPORATION OF THE STATE OF DELAWARE, UNITED STATES OF AMERICA**
	Street Name & Number	**8000 SOUTH FEDERAL WAY BOISE, IDAHO 83707-0006, U.S.A.**
	City	
	State	
	Country	**U.S.A.**
	(b) Name	
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	
	(c) Name	
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	

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III. Declaration of Priority (see note 3)	*Country/Country Designated*	**N.A.**			
	Filing Date				
	Country/Country Designated		*File no.*		
	Filing Date				
	Country/Country Designated		*File no.*		
	Filing Date				

IV. Inventors (See note 4)		
(a) The applicant(s) is/are the sole/joint inventor(s).	[ ] *Yes* [X] *Yes*	[X] *No* [ ] *No*
(b) A statement on Patents Form 8 is/will be furnished.		

V. Name of Agent (if any) (See note 5)	**ARTHUR LOKE BERNARD RADA & LEE**			
VI. Address for Service (See note 6)	*Block/Hse No*		*Level No*	
	Unit No/PO Box	**23-01**	*Postal Code*	**038989**
	Street Name	**9 TEMASEK BOULEVARD #23-01**		
	Building Name	**SUNTEC TOWER TWO**		
VII. Claiming an earlier filing date under section 20(3), 26(6) or 47(4). (See note 7)	*Application No*	**N.A.**		
	Filing Date			

[Please tick in the relevant space provided]:

( ) Proceeding under rule 27(1)(*a*).
Date on which the earlier application was amended = _____
or
( ) Proceeding under rule 27(1)(*b*).

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VIII. Invention has been displayed at an International Exhibition (See note 8)	☐ *Yes* ☒ *No*
IX. Section 114 requirements (See note 9)	The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty. ☐ *Yes* ☒ *No*

X. Check List

(To be filled in by applicant or agent)

A. The application contains the following number of sheet(s):-

1. Request	4	*sheets*
2. Description	11	*sheets*
3. Claim(s).	9	*sheets*
4. Drawing(s).	5	*sheets*
5. Abstract.	1	*sheets*

B. The application as filed is accompanied by:-

1. Priority document		
2. Translation of priority document		
3. Statement of Inventorship & right to grant	X	
4. International Exhibition Certificate		

XI. Signature(s)

(See note 10)

Applicant (a)	
Date	6 August 2001
Applicant (b)	
Date	
Applicant (c)	
Date	

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NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the prescribed fee and 3 copies of the description of the invention, and of any drawings.

2. Enter the name and address of each applicant in the spaces provided at paragraph II. Names of individuals should be indicated in full and the surname or family name should be underlined. The names of all partners in a firm must be given in full. The place of residence of each individual should also be furnished in the space provided. Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided. Where more than 3 applicants are to be named, the names and address of the fourth and any further applicants should be given on a separate sheet attached to this form together with the signature of each of these further applicants.

3. The declaration of priority at paragraph III should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under the Patents (Convention Countries) Order] should be identified and the name of that country should be entered in the space provided.

4. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph IV should be completed by marking the 'YES' Box in the declaration (a) and the 'NO' Box in the alternative statement (b). Where this is not the case, the 'NO' Box in declaration (a) should be marked and a statement will be required to be filed on Patents Form 8.

5. If the applicant has appointed an agent to act on his behalf, the agent's name should be indicated in the spaces available at paragraph V.

6. An address for service in Singapore to which all documents may be sent must be stated at paragraph VI. It is recommended that a telephone number be provided if an agent is not appointed.

7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified at paragraph VII and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(*a*), they should also indicate the date on which the earlier application was amended.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' Box at paragraph VIII should be marked. Otherwise the 'NO' Box should be marked.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' Box at paragraph IX should be marked. Otherwise the 'NO' Box should be marked.

10. Attention is drawn to rules 90 and 105 of the Patent Rules. Where there are more than 3 applicants, see also Note 2 above.

11. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least 2 months after the application has been filed in Singapore.

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Application Filing Date: / /

Request received on : / /

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QUAD FLAT NO-LEAD (QFN) GRID ARRAY PACKAGE, METHOD OF MAKING AND MEMORY MODULE AND COMPUTER SYSTEM INCLUDING SAME

BACKGROUND OF THE INVENTION

[0001] Field of the Invention:

The present invention relates generally to semiconductor packaging. More specifically, the present invention relates to semiconductor packaging using a quad-flat package design incorporating a lead frame and providing an increased number of input/output contacts arranged in a grid array.

[0002] State of the Art:

Conventional quad flat packages (QFP) are formed with a semiconductor die connected to a lead frame and being encapsulated to form a package such that a plurality of leads extends laterally outwardly from each side of the periphery of the encapsulating structure. Such a configuration is relatively simple in design and may be efficiently produced. However, the QFP-type semiconductor has shown various design and production limitations. For example, reducing the overall package size of a QFP becomes difficult because of the arrangement of leads about the lateral periphery of the package. This is particularly evident when reduced package size is attempted to be combined with increasing the number of input/output (I/0) connections required for the smaller yet ever more complex dice representing the state of the art.

[0003] In order to either reduce the size of a conventional QFP while at least maintaining, if not increasing, the number of connections or to increase the number of I/O connections while at least maintaining, if not decreasing, the package size, a higher density of connections would be required along the package perimeter. However, such an increased density of leads about the package perimeter inherently requires a reduced pitch or spacing between adjacent leads and promotes an increased likelihood of cross-talk and signal interference as well as making such packages more difficult to fabricate.

[0004] In an effort the increase the number of connections in an integrated circuit (IC) package while maintaining or decreasing the overall size, alternative packaging arrangements have been implemented. For example, grid array devices such as pin grid arrays (PGA's), ball grid arrays (BGA's), land grid arrays (LGA's) and their associated variants have been used to

reduce package size while and increase input/output connections. As an example of a grid array type device, a BGA device employs a number of input/output connections in the form of conductive bumps, such as solder balls, extending transversely from a major surface of the package in a pattern, or "array,"of columns and rows. The conductive bumps may be formed on one surface of a circuit board or other interposer substrate and are in electrical connection with bonding pads on the opposing surface of the circuit board. A semiconductor die is coupled to the bonding pads, such as by wire bonding, to establish electrical connections from the bond pads of the semiconductor die to the conductive bumps. The resulting assembly is then typically encapsulated such as by transfer molding with a filled polymer with the array of conductive bumps being left exposed for subsequent electrical connection to higher level packaging such as a carrier substrate. The conductive bumps are configured to be coupled to a mirror image pattern of terminal pads on the carrier substrate which may comprise a printed circuit board (PCB) or another structure by reflowing the solder. In essence, a BGA device increases the number of input/output connections by allowing the connections to be positioned over substantially the entirety of a major surface of the package rather than extending laterally outwardly from the periphery of the package such as in a QFP.

[0005] While BGA and other grid array devices provide an increased number of input/output connections and may allow a simultaneous reduction in size for a given package, such devices are not without their own limitations and drawbacks. For example, the use of circuit board interposers, upon which the array of conductive elements is formed, imposes limitations on the size of the package since the circuit board is typically larger than the semiconductor die. Additionally, the circuit boards used in making BGA packages have been known to take on moisture during the fabrication process leading to subsequent cracking and warpage which ultimately renders the device unusable. Furthermore, the cost of circuit boards used in the fabrication of grid array type devices may also may also be viewed as a drawback.

[0006] In view of the shortcomings in the art, it would be advantageous to provide a semiconductor die package which allowed for a higher density of input/output connections without increasing package size. It would further be advantageous to provide such a package having a patterned array of input/output connections formed from a lead frame.

[0007] Additionally, it would be advantageous to provide a method of producing such a package, and the lead frame utilized such a package, which does not require significant changes in tooling or fabrication processes such that the method is easily and efficiently implemented without incurring significant capital costs for new equipment or an increase in process steps.

BRIEF SUMMARY OF THE INVENTION

[0008] One aspect of the invention includes a method of forming a semiconductor die or integrated circuit package. The method includes providing a semiconductor die having a plurality of bond pads located on an active surface thereof. A lead frame having a plurality of conductive leads is provided adjacent the semiconductor die. A first bond bad on the semiconductor die is electrically coupled to a first portion of at least one conductive lead and a second bond pad is coupled to a second portion of the same lead. The first portion and second portion of the lead are then electrically isolated from one another to form two individual conductive elements from the original conductive lead. Additionally, an insulative encapsulant may be formed about the semiconductor die and at least partially about the lead frame while allowing a portion of each individual conductive element to remain exposed for subsequent electrical coupling with an external electrical circuit such as a carrier substrate.

[0009] The individual conductive elements may, for example, be electrically isolated from one another by saw cutting the conductive lead subsequent to the first and second portion being coupled to the bond pads of the semiconductor die. Also, a severance region may be predefined in the lead between the first portion and second portion so as to help facilitate the electrical isolation of the two portions. The severance region may include a notch or recess formed by scoring, cutting or etching partially through the material of the lead. Encapsulant covering the semiconductor die may be extended into the notch or recess of the severance region prior to isolating the first portion and second portion to help retain the first portion and second portion in their respective positions once they have been separated from one another by complete removal of any intervening lead material.

[0010] Another aspect of the present invention includes a method of forming an array of electrically conductive elements for an integrated circuit package. The method includes disposing a semiconductor die having a plurality of bond pads on an active surface thereof on a

lead frame including a plurality of leads. At least two bond pads of the semiconductor die are electrically coupled with each lead of the lead frame. The leads are then severed between the locations of coupling to form at least two electrically isolated conductive elements, each such electrically isolated conductive element being coupled to an individual bond pad on the semiconductor die.

[0011] The present invention also includes a lead frame of a first design. The lead frame includes a plurality of individual leads. At least one of the plurality of leads includes a first bonding region, a second bonding region and a severance region located between the first and second bonding regions. The severance region is configured to facilitate separation of the first bonding region from the second bonding region subsequent to connection of bond pads of a semiconductor die to the respective first and second bonding regions and encapsulation of the lead frame and semiconductor die to form an integrated circuit package.

[0012] The present invention further includes a lead frame of a second design. This lead frame includes a die paddle configured for attachment of a semiconductor die thereto. The lead frame also includes a plurality of conductive elements each having at least two bonding regions. The bonding regions are arranged in a grid array pattern which includes a first peripheral row of bonding regions spaced about a periphery of the die paddle and at least one other peripheral row of bonding regions spaced laterally outwardly from the first peripheral row.

[0013] Yet another aspect of the invention includes a semiconductor die or integrated circuit package. The integrated circuit package includes a semiconductor die, a lead frame and an electrically insulative encapsulant. The lead frame includes a plurality of spaced conductive elements arranged in an array including a first set of conductive elements on a major surface of the package and adjacent a lateral periphery thereof and at least one other set of conductive elements inwardly adjacent the first set. The insulative encapsulant extends over the semiconductor die and at least partially over the lead frame while allowing a portion of each of the conductive elements to be exposed on the major surface for connection with an external electrical circuit. At least one concavity or other recess is defined between and electrically isolates at least one conductive element of the first set and an adjacent conductive element of the at least one other set.

[0014] In accordance with another aspect of the invention another integrated circuit package is provided. The integrated circuit package includes a semiconductor die having a plurality of bond pads and a lead frame having a plurality of conductive leads. Each of the plurality of leads is electrically coupled to at least two bond pads of the plurality of bond pads.

[0015] In accordance with another aspect of the present invention a memory module is provided. The memory module includes a carrier substrate in the form of a module board configured to be electrically coupled to another, higher level packaging structure such as a motherboard, enabling the memory module to communicate with a processor. At least one integrated circuit package having features such as those described above is electrically coupled to the module board.

[0016] In accordance with another aspect of the invention, a computer system is provided. The computer system comprises an input device, an output device, a processor coupled to the input and output devices, and a memory module, such as described above, coupled with the processor.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

[0018] FIG. 1 is a plan view of the bottom of an IC package according to one embodiment of the present invention;

[0019] FIG. 2 is a cross-sectional view of the IC package of FIG. 1;

[0020] FIGS. 3A and 3B are enlarged views of the section specified in FIG. 2 at various stages of manufacturing;

[0021] FIGS. 4A and 4B are plan views of an IC package according to alternative embodiments;

[0022] FIG. 5 is a plan view of a lead frame strip according to one embodiment of the present invention; and

[0023] FIG. 6 is schematic of a computer system incorporating the IC package of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0024] FIGS. 1 and 2 depict one embodiment of an integrated circuit package of the present invention in the form of a quad flat no-lead (QFN) grid array package 10. FIG. 1 presents a view of a major surface comprising the underside of the QFN package 10, while FIG. 2 shows a cross section of the QFN package 10 taken along section line 2-2 as shown in FIG. 1. The QFN package 10 includes a semiconductor die 12 positioned on and secured by its back side to a die paddle 14, die paddle 14 originally comprising a portion of a lead frame as will be hereinafter described. Conductive elements 16 are positioned about the die paddle 14 in a grid array pattern, outwardly of semiconductor die 12 and adjacent the lateral periphery of QFN package 10. The die paddle 14 and conductive elements 16 may be formed of any suitable material such as copper, aluminum, alloy 42 or any other suitable conductive material for lead frames as understood by those of ordinary skill in the art.

[0025] The grid array pattern of the conductive elements 16 may be described in various geometrical terms such as a grid having a specified number columns and rows. However, due to the general placement of the conductive elements 16 outwardly of the semiconductor die 12 and generally adjacent the periphery of the QFN package 10, the grid array structure will be discussed in terms of peripheral rows. Thus, the QFN package 10 shown in FIG. 1 and 2 includes a first inner peripheral row 18A and a second outer peripheral row 18B of conductive elements 16.

[0026] The language "peripheral row" is used herein for convenience in describing the configuration of the QFN package 10 and should not be understood as requiring all of the conductive elements 16 to be located at or on the peripheral edge of the QFN package 10, nor should such phraseology be taken to mean the that a given peripheral row of conductive elements 16 must circumscribe the entire die paddle 14 and semiconductor die. While it is desirable to have the conductive elements 16 positioned about each side of the QFN package 10 so as to maximize the number of conductive elements 16 in the package, some designs may not require such an arrangement. Alternatively, some configurations may include peripheral rows that only partially circumscribe the die paddle 14 and semiconductor die 12, such as arrangements where peripheral rows lie on opposing sides of the QFN package 10.

[0027] The conductive elements 16 are each conductively coupled to a bond pad 22 on the active surface of semiconductor die 12 such as by wire bonds 24. The semiconductor die 12 and wire bonds 24 are encapsulated with an electrically insulative (dielectric) material 26 which also partially encapsulates the conductive elements 16, extending between die paddle 14 and the inner peripheral row 18A of conductive elements 16, between the inner peripheral row 18A of conductive elements 16 and the outer peripheral row 18B of conductive elements 16 and between laterally adjacent conductive elements 16 of each of the peripheral rows 18A and 18B. The encapsulant material 26 may comprise a silicon particle-filled polymer encapsulant applied under heat and pressure by transfer molding, as well known in the art.

[0028] The conductive elements 16 each have an exposed surface 28 on the bottom major surface of the QFN package 10 for subsequent electrical coupling with another electrical component such as a carrier substrate (not shown). Such connection may be made, for example, through the use of conductive bumps 28b, shown in broken lines for clarity. Such bumps may include, for example, solder bumps which are stenciled onto conductive elements 16 and then reflowed to form balls, conductive or conductor-filled epoxy columns or pillars, or self-supporting spheres (either conductive or insulative) covered with a conductive material. It is further contemplated that an anisotropic, so-called "Z-axis" conductive material comprising laterally-spaced conductive elements in a dielectric film and oriented transversely to the plane thereof may also be employed to connect conductive elements 16 to a carrier substrate. All of the foregoing approaches, and others, are known to those of ordinary skill in the art and are not to be taken as limiting of the present invention.

[0029] The inner peripheral rows 18A and outer peripheral rows 18B of conductive elements 16 adjacent each edge of QFN package 10 are shown to be separated from one another by an elongated, trough-like concavity or recess 30. As shown in FIG. 2, the concavity or recess 30 is formed as an elongated saw cut or scribe line extending from a first lateral edge of the QFN package 10 to an opposing lateral edge. However, the concavity may be formed according to other techniques known in the art such as, for example, a masking and etching process. In the embodiment shown in FIGS. 1 and 2, the concavity or recess 30 serves to create the individual conductive elements 16 of the two peripheral rows 18A and 18B from a single row of individual, laterally extending leads of a lead frame. The fabrication process can be seen more clearly with

reference to FIGS 3A and 3B. FIG. 3A depicts a partial section of the QFN package 10 showing the QFN package 10 at a stage in fabrication prior to formation of the individual conductive elements 16. The QFN package shown in FIG. 3A includes a single lead 16' rather than individual conductive elements 16. It is further noted that there are multiple wire bonds 24 connected to different bonding regions 32, 34 of the lead 16'. A severance region 36, shown as an upward-facing notch, is preformed in the lead 16' and subsequently filled with encapsulant 26 subsequent to attachment of semiconductor die 12 to die paddle 14 and wire bonding of a bond pad 22 (not shown in FIG. 3A) to bonding regions 32, 34. The notch of severance region 36 may be formed by various processes such as saw cutting, scribing, scoring or etching of the lead 16' prior to encapsulation of the lead 16' and wire bond 24 and preferably prior to attachment of semiconductor die 12 to die paddle 14.

[0030] Subsequent to the application of encapsulant 26 the lead 16' may be severed, such as through the aforementioned saw cutting or etching, to form individual, electrically isolated conductive elements 16 as shown in FIG. 3B. Each conductive element 16 is connected to a wire bond 24 and thus to a bonding pad 22 of the semiconductor die 12. It is noted that the severance region 36 serves various purposes. First, the severance region 36 identifies an area of separation on the lead 16'. This helps to identify the individual bonding regions 32, 34 during wire bonding of the lead 16' to the bond pads 22 of the semiconductor die 12. Additionally, the severance region 36 allows for the formation of a more shallow concavity or recess 30 during the separation of the lead 16' into individual conductive elements 16, such as to minimize the potential for damage to QFN package 10. Also, by forming the upward-facing notch in the severance region 36 prior to encapsulation, the transfer-molded encapsulant 26 flows under pressure into the notch and substantially laterally about at least three sides of the ultimate location of each conductive element 16 to form a structural member 38 between and about the locations of individual conductive elements 16 to more effectively tie the conductive elements 16 to encapsulant 26, precisely fixing their locations and enabling the package to withstand the stresses placed on leads 16' without damage thereto or movement thereof.

[0031] While the severance region 36 is desirably in the form of a notch or recess as shown, it is contemplated that the severance region 36 of the lead 16' may simply be a designated area of separation without a notch or other physical feature. It is noted that in such a case, the

concavity or recess 30 extending upwardly from the bottom major surface of QFN package 10 would penetrate through the entire thickness of the lead 16' and there would be no encapsulant 26 formed between the adjacent inner and outer individual conductive elements 16 to serve as a structural member 38. If desired, a structural member 38 could be formed after the formation of the concavity 30 by filling same with dielectric material regardless of whether or not an upwardly-facing, preformed notch or recess in each lead 16' is used to facilitate the formation of individual conductive elements 16.

[0032] Referring to FIGS. 4A and 4B alternative embodiments are shown with regard to the grid array pattern. FIG. 4A shows the bottom surface of a QFN package 10' having three different peripheral rows 18A, 18B and 18C of conductive elements 16. The conductive elements 16 are formed in a similar manner as described above except that additional severance regions 36 (or notches) would be located in each lead 16' and that there are additional concavities 30 to assist in forming the third peripheral rows 18C.

[0033] FIG. 4B shows the bottom surface of a QFN package 10" also having three peripheral rows 18A',18B' and 18C'. However, in the embodiment of FIG. 4B the conductive elements 16" of the peripheral rows 18A',18B' and 18C' are staggered such that a conductive element 16" in peripheral row 18B' is shifted slightly to one side as compared to an adjacent conductive element 16" in peripheral row 18A'. Similarly, a conductive element 16" in peripheral row 18C' is shifted slightly to one side as compared to an adjacent conductive element 16" in peripheral row 18B'. Such an arrangement is possible by forming a lead frame having leads 16' positioned at an angle other than perpendicular with respect to an adjacent edge of the die paddle 14. The individual peripheral rows 18A',18B' and 18C' are formed in a manner similar to that described above, with elongated, trough-like concavities 30 being formed to ultimately create the individual conductive elements 16". The staggered configuration serves to allow more flexibility in wire bonding configurations and potentially lower bond loop heights due to the lateral staggering of the conductive elements 16. Thus, depending on the angle at which a lead 16' is formed on a lead frame, the offset of one peripheral row relative to another may be controlled and wire bonding configurations may be flexibly designed.

[0034] Referring now to FIG. 5, an exemplary lead frame strip 50 including a plurality of individual lead frames 52 for use in forming QFN packages 10 is shown. The multiple lead

frames 52 are formed in a single, longitudinally extending strip 50 as is known by those of ordinary skill in the art. Each lead frame 52 includes an outer frame portion 52o bearing a die paddle 14 supported substantially in the center thereof by tie bars and multiple inwardly extending, cantilevered leads 16'. A reduced number of leads 16' is shown for clarity, but is not intended to be limiting of the invention. The leads 16' are each formed with a severance region 36, such as a notch or similar recess, for subsequent formation of individual conductive elements 16 from the leads 16'. As discussed above, the severance regions 36 may be formed by various techniques such as scoring, saw cutting, or etching. The severance regions 36 define the locations of the peripheral rows 18A and 18B which will be subsequently formed in the QFN package 10. The lead frames 52 depicted in FIG. 5 are representative of a lead frame 52 which might be used in the formation of a QFN package 10 described in conjunction with FIGS. 1 and 2. Other lead frames of suitable configuration and with similar features would be utilized in forming the QFN packages 10', 10" discussed in conjunction with FIGS 4A or 4B respectively as is understood by those of ordinary skill in the art. In fabricating QFN packages of the present invention, the outer frame portions 52o are severed from the packages to effect electrical isolation of die paddle 14 as well as each set of conductive elements 16 from the outer frame portions 52o, while mutual electrical isolation between the conductive elements 16 formed from each lead 16' is effected by cutting through the leads 16' from the lead surfaces opposite the notches of severance regions 36. To facilitate alignment of the packages for creating the concavities or recesses 30, it is preferred currently that QFN packages 10 be severed from outer frame portions 52o after such concavities or recesses are cut or otherwise formed. If conductive bumps 28b are to be formed or placed on conductive elements 28, it may also be desirable to form or place conductive bumps 28b while QFN packages 10 are still unsevered from lead frame strip 50 to facilitate alignment and handling. **[To the inventors--Please confirm the foregoing statements as to the fabrication process]**

[0035] Referring now to drawing FIG. 6, a schematic of an electronic system 60, such as a personal computer, including an input device 62 (such as a keyboard and mouse) and an output device 64 (such as a display or printer interface) coupled or otherwise in electrical communication with a processor device 66, is illustrated. Processor device 66 is also coupled or otherwise in operable electrical communication such as through traces of a motherboard with one

or more memory modules 68 incorporating a plurality of QFN packages according to the present invention such as 10, 10', 10" or variations thereof. The memory module 68 may include a memory board 70 having an electrical circuit formed therein, such as a PCB. Furthermore, processor device 66 may be directly embodied in a module with a QFN package which incorporates the teachings hereof and further include, without limitation, a microprocessor, a first level cache memory, and additional integrated circuits, such as logic circuits, a video processor, an audio processor, or a memory management processor.

[0036] While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit package comprising:

providing a semiconductor die having a plurality of bond pads on an active surface thereof;

providing a lead frame including a plurality of conductive leads;

electrically coupling a first bond pad of the plurality of bond pads to a first portion of at least one conductive lead;

electrically coupling a second bond pad of the plurality of bond pads to a second portion of the at least one conductive lead; and

electrically isolating the first portion of the at least one conductive lead from the second portion of the at least one conductive lead.

2. The method of claim 1, further comprising encapsulating the semiconductor die and at least a portion of the lead frame in a dielectric material.

3. The method of claim 2, wherein the electrically isolating the first portion from the second portion is effected subsequent to the encapsulating.

4. The method of claim 1, wherein the electrically isolating the first portion from the second portion of the at least one conductive lead includes mechanically severing the at least one conductive lead between the first portion and the second portion.

5. The method of claim 1, wherein the electrically isolating the first portion from the second portion of the at least one conductive lead includes etching to sever the at least one conductive lead between the first portion and the second portion.

6. The method of claim 1, wherein the electrically coupling the first bond pad to a first portion of the at least one conductive lead includes wire bonding.

7. The method of claim 6, wherein electrically coupling the second bond pad to a second portion of the at least one conductive lead includes wire bonding.

8. The method of claim 1, further comprising forming a notched region in a surface of the at least one conductive lead between the first portion and the second portion.

9. The method of claim 8, further comprising encapsulating the semiconductor die and at least a portion of the lead frame including the notched region of the at least one conductive lead in a dielectric material.

10. The method of claim 9, wherein the electrically isolating the first portion from the second portion includes separating the first portion from the second portion while leaving at least some dielectric material in the notched region.

11. The method of claim 10, wherein the separating the first portion from the second portion includes cutting the at least one conductive lead into the notched region from an opposing surface of the at least one conductive lead.

12. A method of forming an array of electrically conductive elements on an integrated circuit package, the method comprising:

securing a semiconductor die having a plurality of bond pads on an active surface thereof to a lead frame having a plurality of leads;

electrically coupling each lead of the plurality of leads at spaced locations with one of at least two different bond pads of the plurality of bond pads; and

severing each lead between the spaced locations to form at least two electrically isolated conductive elements.

13. A lead frame comprising:

a plurality of leads, including at least one lead having:

a first bonding region,

a second bonding region, and

a severance region located between the first bonding region and the second bonding region, the severance region being configured to facilitate separation of the first bonding region from the second bonding region.

14. The lead frame of claim 13, wherein the severance region includes a notch in the lead.

15. The lead frame of claim 13, wherein each of the plurality of leads include a first bonding region, a second bonding region, and a severance region configured to facilitate separation of the first and second bonding regions.

16. The lead frame of claim 15, wherein each severance region includes a notch.

17. A lead frame for an integrated circuit package, the lead frame comprising:

a die paddle configured for attachment to a semiconductor die; and

a plurality of conductive elements each having at least two bonding regions arranged in a grid array about the die paddle, the grid array including at a first peripheral row of bonding regions spaced about a periphery of the die paddle and at least one other peripheral row of bonding regions spaced outwardly from the first peripheral row of bonding regions.

18. An integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die;

an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least

partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

19. The integrated circuit package of claim 18, wherein the semiconductor die includes a plurality of bond pads and wherein each of the plurality of bond pads are electrically connected with a conductive element of the plurality of conductive elements.

20. The integrated circuit package of claim 19, wherein the electrical connection between each of the plurality of bond pads and each respective conductive element of the plurality of conductive elements includes a wire bond.

21. The integrated circuit package of claim 18, wherein the conductive elements of the first set of conductive elements are substantially aligned with the conductive elements of the at one other set transverse to an adjacent outer lateral peripheral edge of the integrated circuit package.

22. The integrated circuit package of claim 21, wherein the conductive elements of the first set of conductive elements are offset relative to the conductive elements of the at one other set.

23. The integrated circuit package of claim 18, wherein the recess comprises an elongated, trough-like recess extending substantially between conductive elements of the first set and conductive elements of the second set disposed along a common laterally outer peripheral edge of the integrated circuit package.

24. A semiconductor die assembly, comprising:

a semiconductor die having a plurality of bond pads;

a lead frame having a plurality of conductive leads, each lead being electrically coupled at spaced locations on the lead to at least two bond pads of the plurality of bond pads.

25. The integrated circuit package of claim 24, further comprising a dielectric encapsulant formed about the semiconductor die and partially about the lead frame.

26. The integrated circuit package of claim 24, further comprising a wire bond coupling each lead at the spaced locations thereon to one of the at least two bond pads of the plurality of bond pads.

27. The integrated circuit package of claim 26, wherein each lead includes a severance region configured to facilitate separation into at least two mutually electrically isolated conductive elements.

28. A memory module comprising:

a module board configured to be electrically coupled with a higher level of packaging; and

at least one integrated circuit package electrically coupled with the module board, the integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die;

an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

29. A computer system comprising:

an input device;

an output device;

a processor coupled to the input and output devices; and

a memory module coupled to the processor, the memory module comprising a module board coupled to at least one integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die;

an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

30. A semiconductor die assembly, comprising:

a semiconductor die having a plurality of bond pads on an active surface thereof;

at least one set of mutually spaced conductive elements laterally outboard of at least one peripheral edge of the semiconductor die, and at least another set of mutually spaced

conductive elements spaced from and laterally outboard of the at least one set of conductive elements;

a plurality of wire bonds extending between bond pads of the plurality and conductive elements of the first and second sets; and

a package comprising dielectric material extending over the semiconductor die and wire bonds and having an outer lateral periphery substantially coincident with outer lateral extents of the at least one other set of conductive elements, dielectric material of the package extending at least partially about each of the conductive elements and leaving a surface thereof exposed.

31. The semiconductor die assembly of claim 30, further comprising a die paddle to which the semiconductor die is secured by a back side thereof.

32. The semiconductor die assembly of claim 30, wherein the at least one set of mutually spaced conductive elements and the at least another set of conductive elements extend around a plurality of peripheral edges of the semiconductor die.

33. The semiconductor die assembly of claim 30, wherein the at least one set of mutually spaced conductive elements and the at least another set of conductive elements extend around four peripheral edges of the semiconductor die.

34. The semiconductor die assembly of claim 30, further including an elongated, trough-like recess extending between conductive elements of the at least one set and conductive elements of the at least another set and substantially parallel to the at least one peripheral edge of the semiconductor die.

35. The semiconductor die assembly of claim 30, wherein the exposed surfaces of the conductive elements are oriented substantially parallel to the active surface of the semiconductor die.

36. A method of fabricating a semiconductor die assembly, comprising:

placing a semiconductor die within a plurality of leads extending laterally outwardly from peripheral edges thereof;

wire bonding bond pads on the semiconductor die to spaced locations on the leads of the plurality;

transfer molding a dielectric encapsulant over the semiconductor die, wire bonds and leads, leaving undersurfaces of the leads exposed; and

severing the leads between the spaced locations.

37. The method of claim 36, further comprising notching upper surfaces of the leads between the spaced locations before the placing the semiconductor die within the plurality of leads.

38. The method of claim 36, wherein the placing the semiconductor die includes securing the semiconductor die to a die paddle located within the plurality of leads.

39. The method of claim 36, wherein the severing is effected by making a linear cut between the spaced locations on each lead extending from a common peripheral edge.

40. The method of claim 39, further comprising notching upper surfaces of the leads between the spaced locations before the placing the semiconductor die within the plurality of leads, and wherein the linear cut is extended substantially only to a depth sufficient to intersect bottoms of the notches so that some dielectric material remains between the spaced locations.

41. A lead frame strip, comprising:

a plurality of longitudinally arranged lead frames, each lead frame including an outer frame portion bearing a plurality of inwardly extending, cantilevered leads, and each lead of the plurality having thereon at least two longitudinally spaced locations separated by a severance region comprising a notch extending laterally across the lead.

42. The lead frame strip of claim 41, wherein each outer frame portion further bears a die paddle substantially centered therein.

43. The lead frame strip of claim 41, wherein the plurality of inwardly extending, cantilevered leads are located on a plurality of sides of each outer frame portion.

44. The lead frame strip of claim 41, wherein the plurality of inwardly extending, cantilevered leads are located on four sides of each outer frame portion.

ABSTRACT

QUAD FLAT NO-LEAD (QFN) GRID ARRAY PACKAGE, METHOD OF MAKING AND MEMORY MODULE AND COMPUTER SYSTEM INCLUDING SAME

A quad flat no-lead (QFN) grid array semiconductor package and method for making the same. The package includes a semiconductor die and a lead frame having conductive elements patterned in a grid-type array. A plurality of bond pads on the semiconductor die are coupled to the plurality of conductive elements, such as by wire bonding. The semiconductor die and a portion of at least a portion of the lead frame are encapsulated in an insulative material leaving the conductive elements exposed along a bottom major surface of the package for subsequent electrical connection with higher level packaging. Individual conductive lead elements, as well as the grid array pattern, are formed by wire bonding multiple bond pads to a single lead at different locations and subsequently severing the leads between the bonding locations to form multiple conductive elements from each individual lead.

[Figure 1]

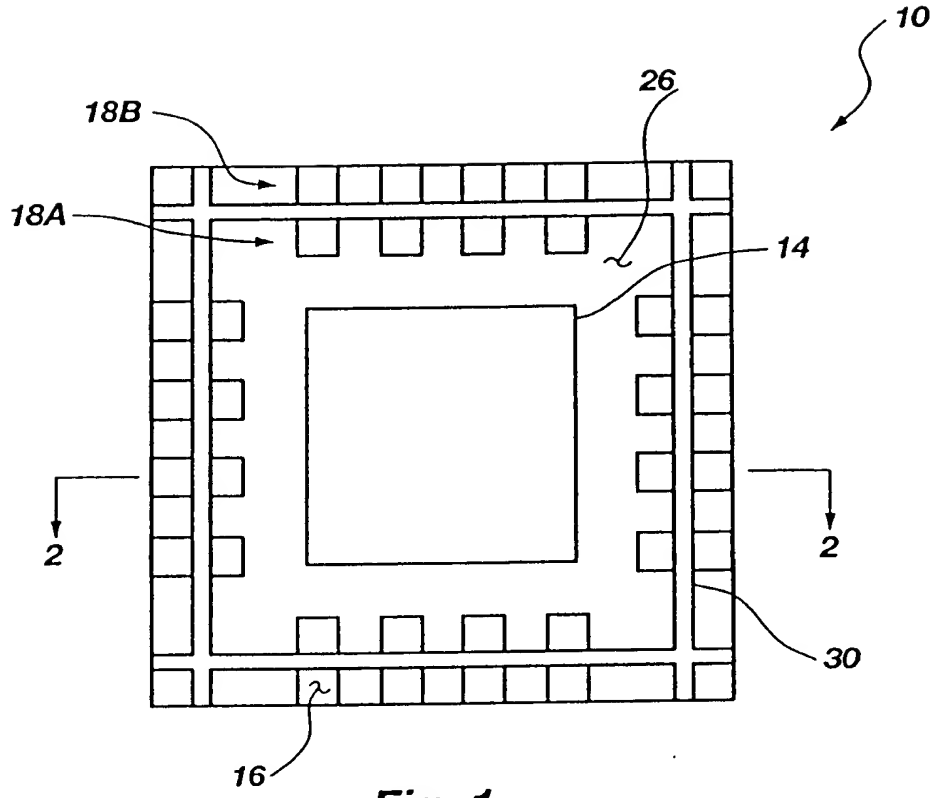
10
26
18B
18A
14
2
2
30
16

Fig. 1

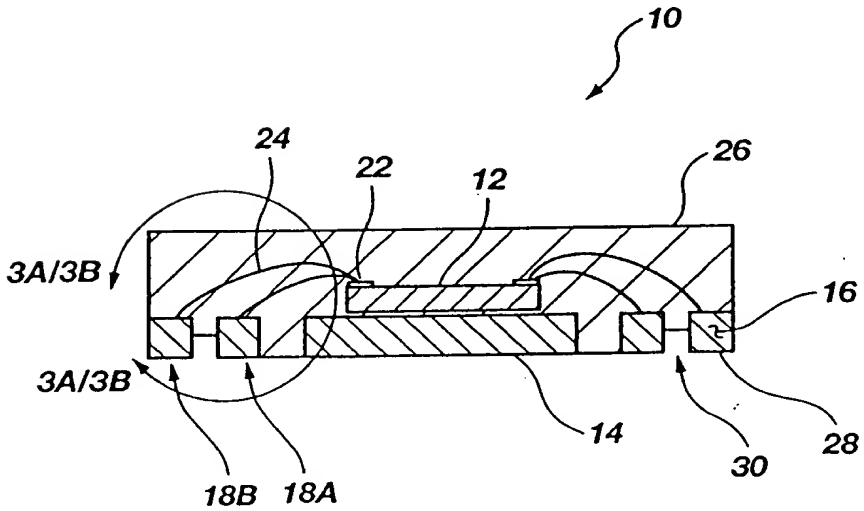
10
24
22
12
26
3A/3B
16
3A/3B
14
28
30
18B
18A

Fig. 2

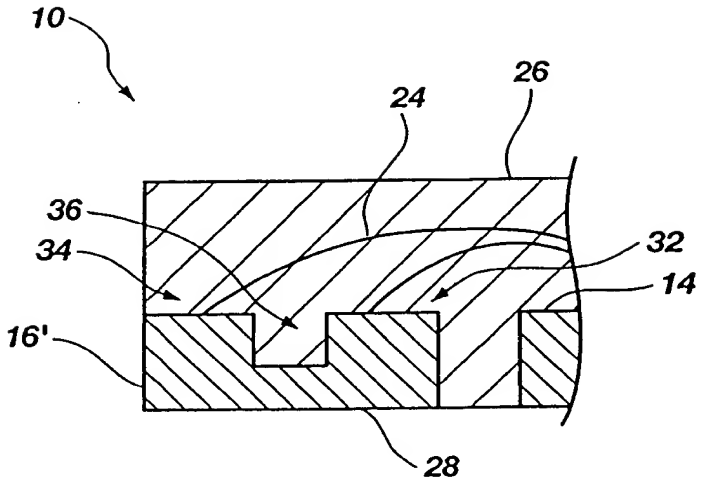

Fig. 3A

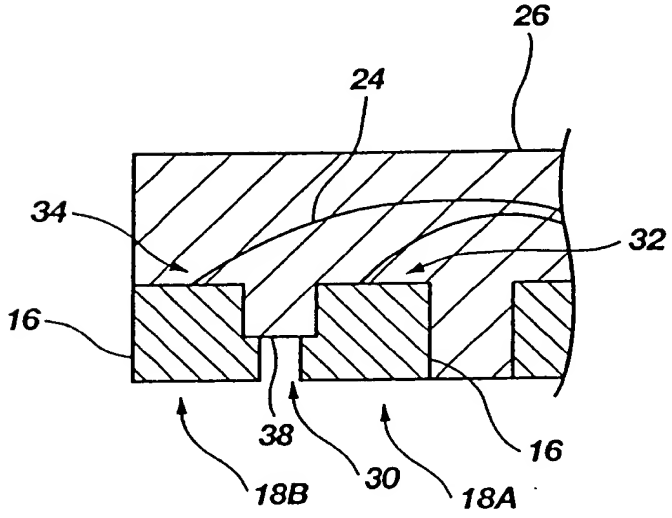

Fig. 3B

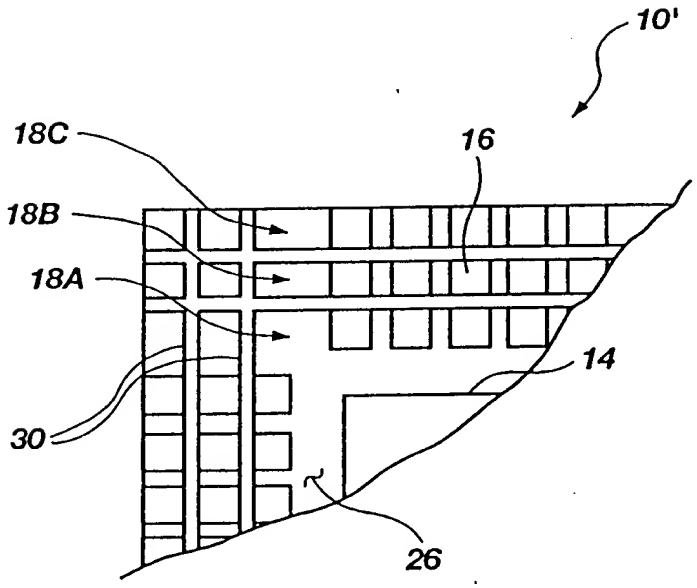

Fig. 4A

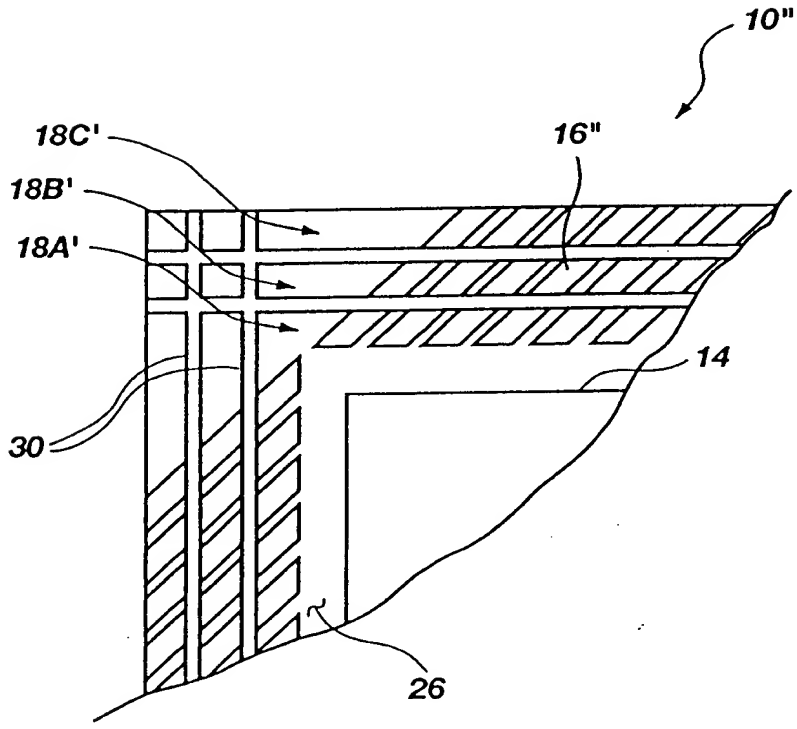

Fig. 4B

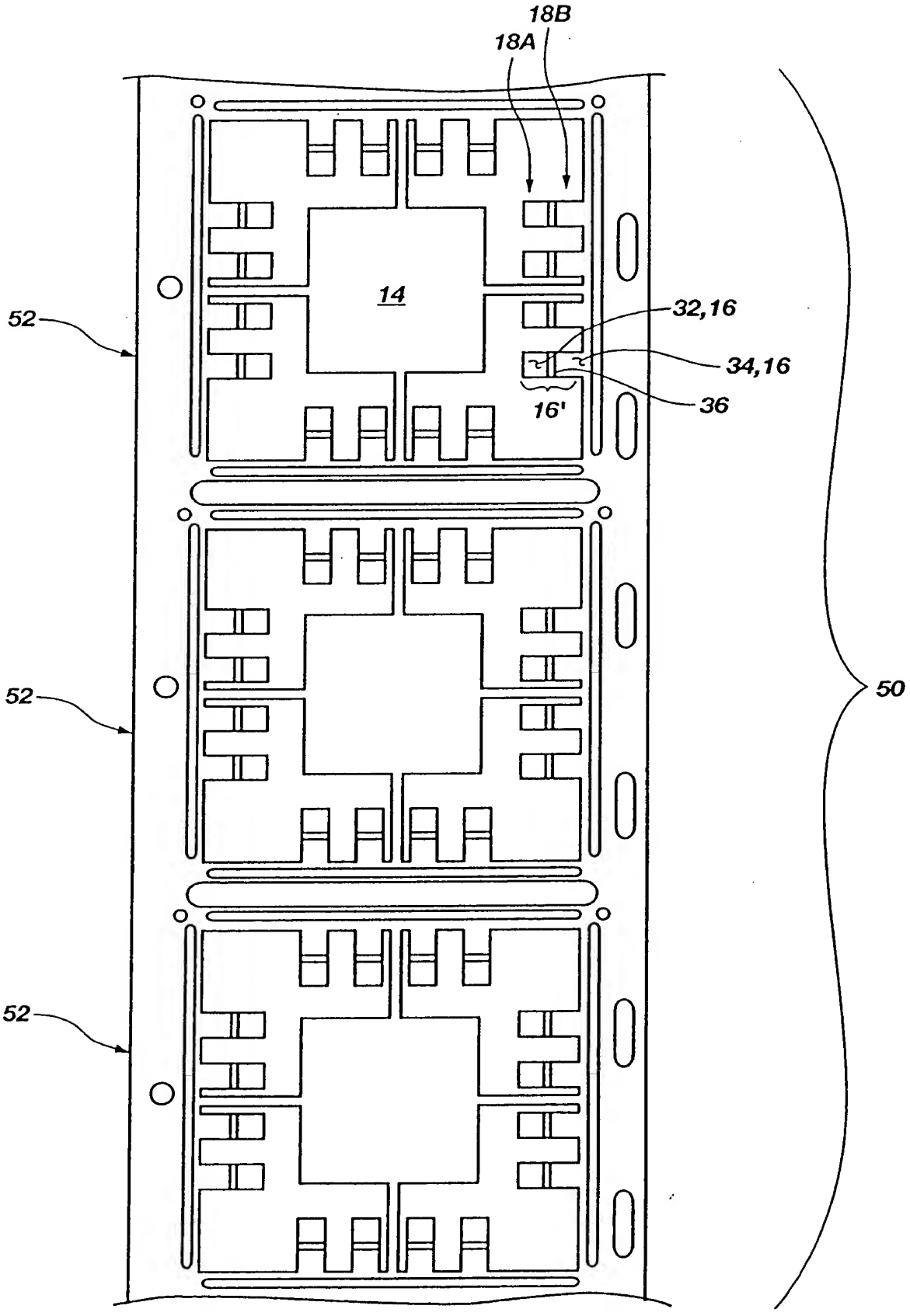

Fig. 5

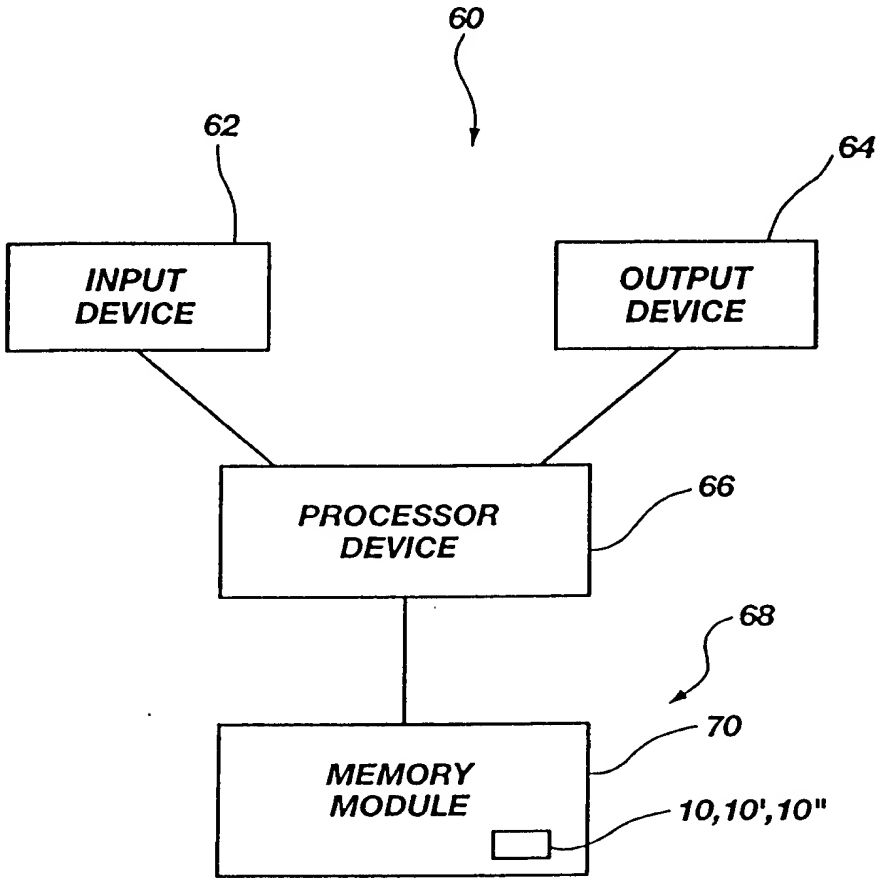
60
62
64
INPUT DEVICE
OUTPUT DEVICE
PROCESSOR DEVICE
66
68
70
MEMORY MODULE
10,10',10"

Fig. 6